Preliminary publication of JEDEC Semiconductor Memory Standard

This Standard was developed by JEDEC Committee JC-42.5 and approved by the JEDEC Board of Directors at their February '03 meeting (#128). It is published here in preliminary form, prior to being published in final form.

1) Title of Standard: Design File Registration Procedure

Council Ballot Number: JCB 03-008

Committee Ballot Number: 42.5-02-287

Committee Item Number: 1367.01

Date of Council Approval: February 2003

Background: At the September JC-42.5 meeting, the design file registration ballot item #1367, JC-42.5-02-199 passed by count. However, the comments noted that the registration process was not well understood, and there was a request to add a registration numbering system. The committee voted to reballot a complete manual for design file registrations. The reballot was issued under JC42.5-02-287 with the new item number #1367.01 and counted in the Dec 2002 meeting. IBM asked to specificly include the requirements that need to be met by the sponsor before a Gerber should be posted and made a detailed counterproposal. This was accepted by the committee as 'editorial refinement' along with other editorial comments. As this is not a device standard but a JC42.5 operating procedure, the BoD will decide how this should be published.

JC42.5-02-287 edited Item #1367.01

JEDEC Module Design Specification Standardization and Design File Registration Process

Purpose:

This document defines the procedure associated with the standardization of new (or modified) module 'Design Specifications' and the registration of the associated module design files.

Definition:

1. Module Design Specifications are documents that provide a written description that fully describe the attributes and objectives for one or more module 'reference designs'
2. Design Files refer to design data associated with specific module designs, and include all information required to produce a module consistent with a specific Module Design Specification. These designs achieve JEDEC Registration once the associated Design Specification is approved by committee and Council voting. Design file Registrations can be modified to fit production processes.

NOTE: A Design File usually represents the module design that was used within the respective task or working group to simulate and assure functionality under certain system assumptions and to derive the respective DIMM specifications. It is one of the many possible implementations of the Design Specification. The Design Specification remains the criteria for conformance. Vendor specific changes are allowed as long as the design specification is met. Registrations can contain JEDEC standardized components such as block diagrams, trace lengths, pinouts, loading etc. These Design Specifications cannot be modified without committee approval (JC-42.5 ballot process). Standards require the approval of the sponsoring committee and the JEDEC Board of Directors (BoD).

Design File Requirements: (To be inserted here:JC-42.5 item #1289, IBM sponsor)

Design Specification Standardization and Design File <u>Registration Procedure</u>:

1. First showing: A company will present a first showing of the design objectives and key attributes to the JC-42.5 committee, either electronically or in person at a committee meeting.
2. Second showing: At the next committee meeting, the sponsoring company will present a second showing.

The second showing must consist of the following information, at minimum. If some of this information is unavailable at second showing, or if it changes prior to voting, the information must be included as 'reference material' at ballot time.

Second showing Content for DIMM Design Standards:

- **Design Objectives**
- **Block Diagram(s)**
- **Net structures**
- **Key support chips (simplified Bill Of Material)**

- **Design & mfg guidelines (cross section, impedance, trace widths/spacings…)**
- **Card outline, keying**
- **Timing Budget and example (RDIMMs only)**
- **Simulation cases analyzed, summarized results (key cases)**
- **Compatibility objectives/summary (to existing design standards, if appropriate)**
- **Evaluation hardware plans/requirements (Clock Reference Board… if applicable)**
- **Location of design files and specification (web site?), contact person**

For additions to current JEDEC Design Specifications, it is necessary to provide only that material that differs from the original material.

3. Voting: After the intended final set of design data has been posted in the committee's member's section, the Design Specification may be voted to ballot at the second showing meeting.
4. Ballot counting: The ballot is counted at the next committee meeting. If the ballot passes Committee and Council voting, the Design Specification will be considered as a JEDEC Standard, the associated Design Files will be considered as JEDEC Registrations, and the design files will be posted on the JEDEC web site.
5. Posting to web: The Design Specification and Design Files will remain on the JEDEC public web site indefinitely. As the JEDEC staff will not be able to provide technical support for the files, the sponsoring company shall provide contact information for support of the files to the JEDEC office.
6. Removal: A committee ballot is necessary to remove the files from the web site.

Registration Naming Guide:

Design files will be named as they are on the JEDEC standard for the file, including the revision number for the design.

Example: DDR Unbuffered DIMM REV. 0.98 Raw card A