

6 APPLICABLE OTHER DOCUMENTS

The following documents are publications which are related to the work of Committee JC-42 and may be obtained from the Electronic Industries Association, Standards Sales Department.

6.1 - Standard Manufacturers Identification Code. JEDEC Publication No. 106A

JEDEC Committee JC-42 maintains a Vendor identification code list for memory device manufacturers. This code number which can be used as a unique numerical identification for a Vendor in documentation, software, or encoded in ROM on a memory device. The list is updated periodically and published as JEDEC publication 106A.

6.2 - Interface Standard for Low Voltage TTL-Compatible Devices (LVTTTL) JEDEC Standard No. 8 and Addendum No. 1

A series of standards have been developed which define the power supply and signal interface limits for devices which operate with a power voltage of three (3.0) volts nominal. It includes tolerances for both battery and regulated power supply operation. The input and output signal limits when operating with 5.0 V

nominal TTL circuits are defined. These standards are intended to define the electrical environment for the device families which will utilize the 3.0 V power supply voltage which, it is expected, will replace the current 5.0 V standard. These standards have been published as JEDEC Standard 8 with Addendum 1.

6.3 - Package Outlines, JEDEC Publication 95

This document contains dimensional drawings of all component packages which have been registered or approved as standards by JEDEC. It is issued in loose leaf binder form into which periodic updates may be added.

6.4 - PLD Data Transfer Format, JEDEC Standard 3-B

This standard defines the format used to communicate the device programming information to a programmer for a field programmable memory device. In addition, it gives a simple transmission protocol to be used for the transmission. Since Standard 3-B was published, an addition to the standard defining a "J" field had been approved.

6.5 - Nomenclature for FPLD, EIA Standard RS-428

This standard defines a compact nomenclature to be used to describe Field Programmable Logic Devices. The standard is applicable to all current and future devices, regardless of technology, density, and package. The details of the standard will be published as an addendum to EIA Standard RS-428.

6.6 - DDR SDRAM Device Specification Standard, JESD79

This Standard defines all architectural and performance parameters that are needed to define a family of DDR SDRAM devices. It is also referenced in Sec. 3.20.1

6.7 - DDRII SDRAM Device Specification Standard, JESD79-2

This Standard defines all architectural and performance parameters that are needed to define a family of DDRII SDRAM devices.

6.8 - DDRIII SDRAM Device Specification Standard, JESD79-3

This Standard defines all architectural and performance parameters that are needed to define a family of DDRIII SDRAM devices.

6.9 - SPECIALITY DDR2-1066 SDRAM , JESD208

This Standard defines all architectural and performance parameters that are needed to define a family of Specialty DDR2-1066 SDRAM devices.

6.10 - LOW POWER DOUBLE DATA RATE (LPDDR) SDRAM STANDARD , JESD209

This Standard defines all architectural and performance parameters that are needed to define a family of LPDDR SDRAM devices.