3.1 General Standards

The following standards are applicable to multiple technologies and functionalities but are presented as a single family of devices.

3.1.1 Bytewide

The devices in the following sections have an 8 bit (byte) wide data interface. All devices are Type B unless otherwise stated.

3.1.1.1 - 32K TO 256K BY 8 A/A MX FAMILY IN DIP

CAPACITY--32K, 64K, 128K, 256K WORDS OF 8 BITS
LOGIC FEATURES--Multiplexed Address
PACKAGE--24 PIN DIP, 0.4“ WIDE
PIN ASSIGNMENT--Fig. 3.1-1

This standard defines the generalized pin assignments for a family of address multiplexed byte wide memory devices. Specific pinout variations for different technologies will be defined at a later time.